AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A memory controller comprising:

means for receiving, from a processor, a request for access to a single dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for activating a first page to be accessed, based on said access request from said processor, and executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of said second page to be accessed subsequently,

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

2. (Currently Amended) A memory controller comprising:

means for receiving, from a processor, a request for access to a single dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for activating a first page to be accessed, based on said access request from said processor, and executing, before a next request for access to a second page to be accessed subsequently by said processor, precharge of a bank corresponding to said second page to be accessed subsequently,

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

3. (Currently Amended) A memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal adapted to receive a request for access from said processor to a single dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for issuing an active command for activating a first page to be accessed, based on said access request from said processor, and issuing a precharge command for executing, before a next request for access to a second page to be accessed subsequently, precharge of said second page to be accessed subsequently,

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks .

4. (Currently Amended) A memory controller for use with a processor and a dynamic random access memory, comprising:

a terminal adapted to receive a request for access from said processor to a single dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

memory control means for issuing an active command for activating a first page to be accessed, based on said access request from said processor, and

issuing a precharge command for executing, before a next request for access to a second page to be accessed subsequently, precharge of a bank corresponding to said second page to be accessed subsequently,

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

5. (Currently Amended) A memory controller comprising:

a terminal adapted to receive, from a processor, a request for access to a single dynamic random access memory having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

a memory control unit adapted to activate a first page to be accessed, based on said access request from said processor, and to execute, before a next request for access to a second page to be accessed subsequently by said processor, precharge of said page to be accessed subsequently,

wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks.

6. (New) A memory controller according to claim 1, wherein said memory control means includes means for executing a precharge of said second page during a time period between a read operation of said first page and the request for access to the second page.

7. (New) A memory controller according to claim 2, wherein said memory control means includes means for executing a precharge of said bank corresponding to said second page during a time period between a read operation of the first page and the request for access to the second page.

8. (New) A memory controller according to claim 6, wherein said memory control means includes means for executing a precharge of said second page during a time period between a read operation of said first page and the request for access to the second page.

9. (New) A memory controller according to claim 4, wherein said memory control means includes means for executing a precharge of said bank corresponding to said second page during a time period between a read operation of the first page and the request for access to the second page.

10. (New) A memory controller according to claim 5, wherein said memory control means includes means for executing a precharge of said second page during a time period between a read operation of said first page and the request for access to the second page.